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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,053	11/18/2003	Bruce G. Hazelzet	BUR920020085US1	1052

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IBM MICROELECTRONICS
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EXAMINER

TRAN, MICHAEL THANH

ART UNIT	PAPER NUMBER
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2827

NOTIFICATION DATE	DELIVERY MODE
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06/03/2009

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 10/707,053	Applicant(s) HAZELZET ET AL.	
	Examiner MICHAEL T. TRAN	Art Unit 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 January 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4,6,8-10 and 12-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1,2,4,6,8-10 and 12-14 is/are allowed.
- 6) ☒ Claim(s) 15-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. In response to the Communications dated January 15, 2009, claims 1, 2, 4, 6, 8-10 and 12-17 are active in this application.

Specification

2. If there are cross-reference to related applications, please include the respective patent numbers, if known.

Claim Objections

3. It appears that the phrase "the plurality of DRAMs", in claim 16, lacks antecedent basis.

In claim 17, the phrase "maybe" renders the claim indefinite. Does the device actually does what it is claimed?

In claim 10, the word "may" renders the claim indefinite. Does the device actually does what it is claimed?

Claim Rejections- 35 U.S.C. § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-

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(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

5. Claim 16 is rejected under 35 U.S.C 102(b) as being anticipated by Morishima [U.S. Patent Application #20020064075].

With respect to claim 16, Morishima disclose, in figures 1-3, a computer system with a memory system comprising: memory devices and re-drive circuitry [3] external to the said memory devices, said re-drive circuitry adapted to invert an address [YO] or command input signal subsequently output to one or more of the plurality of DRAMs [MA's] via a programmable input [input electrodes], such that simultaneous switching noise is reduced inverted signals based on a selected operation mode [inherent – see Summary of Invention, paragraph 0047].

6. Claim 17 is rejected under 35 U.S.C 102(b) as being anticipated by Morishima [U.S. Patent Application #20020064075].

With respect to claim 17, Morishima discloses, in the figures, a memory module, comprising: a plurality of memory devices [M1-Mn, L1-L4 and CG1-CG4] each having a plurality of programmable address and control inputs that are configured by a plurality of programmable pins [electrodes] each dedicated to one of the plurality of memory devices, such that the plurality of memory devices may be individually programmed to receive non-inverting or inverting inputs [via 5/4/3/6 - it is noted that elements 3-6 are being interpreted as one element]; and a plurality of registers [5/4/3/6] integral to the memory

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module, each programmed to output to a corresponding one of the plurality of memory devices, at least a portion of received address [Y0] and command signals [WE] as non-inverted or inverted [see figure 5] in response to received address or command inputs, such that normal operation of the plurality of memory devices is maintained.

Claim Rejections - 35 U.S.C. § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Dell et al. [U.S. Patent # 5,513,135] in view of Itou [U.S. Patent # 5,999,483].

Dell et al. disclose DIMM comprising: a module having plurality of DRAMs [see specification – it is noted that Dell et al. also stated that DRAMs and SDRAMs are interchangeable].

Itou discloses all of the above mentioned but is silent about the internal elements of the SDRAM device. However, this is not new. Itou disclose DRAMs with means for operating with non-inverted or inverted signals based on a pre-selected operating mode [see figure 2]; and signal re-drive circuitry [output of one inverter inputting to another inverter] adapted to invert an address or command input signal subsequently output to one or more of the plurality of DRAMs, wherein an output mode of the signal re-drive circuitry is responsive to a programmable input [controller]. Therefore, it would have been obvious

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to one having ordinary skill in the art at the time the invention was made to modify the Dell et al. memory circuit element to include the element as taught by Itou, since the modification is merely a substitution of a functionally recognized equivalent element.

Remarks

9. Applicant's arguments filed January 15, 2009 have been fully considered but they are not persuasive.

With respect to claim 16, Applicant argued that the Morishima reference does not disclose a memory system capable of receiving either non-inverted or inverted signals, nor does it disclose external re-drive circuitry to selectively output non-inverted or inverted outputs. However, it is noted that the Examiner is broadly interpreting the claim language. In the claim, the recitation claims "memory devices", this maybe interpreted as being the plurality of any element within the figures – for example, buffers, decoders or drivers. The recitation further claims "re-drive circuitry" to selectively output non-inverted or inverted outputs, this maybe interpreted as being the 5c-5f elements which receive Y0 and it's inverted form via 5a. Additionally, the recitation of the plurality of DRAMs maybe interpreted as being the plurality of "M1-Mn" in the figures. Furthermore, since Morishima indicated that the application of their invention is to suppress noise; hence, the recitation of noise reduction in the claim is met.

With respect to claim 15, Applicant's arguments did not appear to address the specifics of the rejection of the claim, therefore, claim 15 stands rejected. Further, Applicant stated that the Dell and Itou references are not combinable since they are directed to two separate inventions. However, it is noted that both are directed specifically towards DRAMs. Hence, it is reasonable to combine the two references.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH

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shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

Allowable Subject Matter

10. Claims 1, 2, 4, 6, 8-10 and 12-14 are allowable over the prior art of record.

11. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- programmable pins in the register and the DRAMs to enable operation in either non-inverted or inverted mode, wherein a first programmable pin is connected to ground to enable an inverting mode and a second programmable pin is connected to Vdd to operate in a non-inverting mode.
- a memory controller capable of enabling the plurality of DRAMs to accept either non-inverted or inverted signals using a programmable pin, which dynamically configures the polarities of address and command signals exchanged between a plurality of signal drivers and the plurality of DRAMs, such that simultaneous switching noise in the memory system is reduced.
- non-inverted input signals and inverted input signals, wherein pre-selected DRAMs may operate in the inverted mode with some critical signals remaining in a non-inverted mode; a means connected to the circuits for changing modes to accept inverted input signals; and a memory controller which is programmable to operate in non-inverted mode at power up and to change after it is programmed.

Conclusion

12. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

13. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

14. Any inquiry of a general nature or relating to the status of this application.

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should be directed to the Group receptionist whose telephone number is (571) 272-1650.

/Michael T. Tran/
Michael T. Tran
Art Unit 2827
June 1, 2009